WHAT IS CLAIMED IS:

1. For use in a processor having separate instruction and data buses, separate instruction and data memories and separate instruction and data units, a mechanism for supporting self-modifying code, comprising:

a crosstie bus coupling said instruction bus and said data unit; and

a request arbiter, coupled between said instruction and data units, that arbitrates requests therefrom for access to said instruction memory.

2. The mechanism as recited in Claim 1 wherein said data unit can employ said instruction memory to contain data.

3. The mechanism as recited in Claim 1 wherein said request arbiter gives a higher priority to requests from said data unit.

4. The mechanism as recited in Claim 1 further comprising an instruction prefetch mechanism that prefetches instructions from a said instruction memory into an instruction cache, said request arbiter stalling said prefetch mechanism when said request arbiter grants a request from said data unit for said access to said instruction memory.

5. The mechanism as recited in Claim 3 wherein at least some instructions prefetched into said instruction cache are invalidated when said request arbiter grants said request.

6. The mechanism as recited in Claim 4 wherein a programmable control register is employed to invalidate said at least some instructions.

7. The mechanism as recited in Claim 1 wherein said instruction memory is a local instruction memory and said processor further comprises an external memory interface.

8. The mechanism as recited in Claim 1 wherein said processor is a digital signal processor.

9. A method of supporting self-modifying code in a processor having separate instruction and data buses, separate instruction and data memories and separate instruction and data units, comprising:

arbitrating requests from said instruction and data units for access to said instruction memory; and

communicating instructions between said instruction bus and said data unit via a crosstie bus extending therebetween.

10. The method as recited in Claim 9 wherein said data unit can employ said instruction memory to contain data.

11. The method as recited in Claim 9 wherein said arbitrating comprises giving a higher priority to requests from said data unit.

12. The method as recited in Claim 9 further comprising:

prefetching instructions from a said instruction memory into an instruction cache; and

stalling said prefetch mechanism when a request from said data unit for said access to said instruction memory is granted.

13. The method as recited in Claim 12 further comprising invalidating at least some instructions prefetched into said instruction cache when said request is granted.

14. The method as recited in Claim 13 wherein a programmable control register is employed to invalidate said at least some instructions.

15. The method as recited in Claim 9 wherein said instruction memory is a local instruction memory and said processor further comprises an external memory interface.

16. The method as recited in Claim 9 wherein said processor is a digital signal processor.

17. A digital signal processor, comprising:

an execution core having an instruction cache;

a memory unit coupled to said execution core and having separate instruction and data buses, separate instruction and data memories and separate instruction and data units;

a crosstie bus coupling said instruction bus and said data unit; and

a request arbiter, coupled between said instruction and data units, that arbitrates requests therefrom for access to said instruction memory.

18. The digital signal processor as recited in Claim 17 wherein said data unit can employ said instruction memory to contain data.

19. The digital signal processor as recited in Claim 17 wherein said request arbiter gives a higher priority to requests from said data unit.

20. The digital signal processor as recited in Claim 17 further comprising an instruction prefetch mechanism that prefetches instructions from a said instruction memory into said instruction cache, said request arbiter stalling said prefetch mechanism when said request arbiter grants a request from said data

unit for said access to said instruction memory.

21. The digital signal processor as recited in Claim 20 wherein at least some instructions prefetched into said instruction cache are invalidated when said request arbiter grants said request.

22. The digital signal processor as recited in Claim 21 wherein a programmable control register is employed to invalidate said at least some instructions.

23. The digital signal processor as recited in Claim 17 wherein said instruction memory is a local instruction memory, said data memory is a local data memory and said memory unit further has an external memory interface.